



HCMOS/TTL COMPATIBLE HIGH STABILITY VCXO IN 14 PIN DIP PACKAGE- VC14H Series

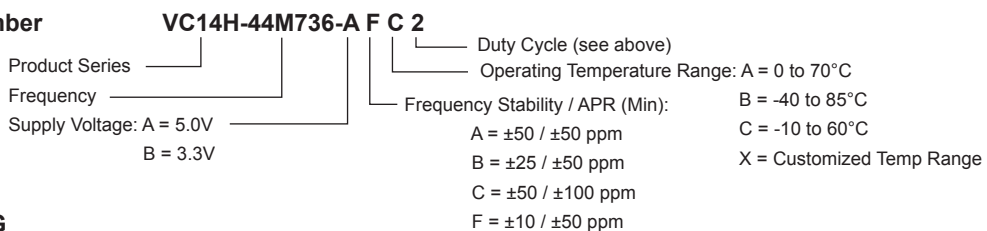
FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Pulling Range, 5 VDC or 3.3 VDC Option
- Very Low Phase Jitter with Fundamental Crystal Design
- Commercial or Industrial Temperature Range, Industry Standard Lead Spacing
- Sealed UM-1 Crystal Inside for High Stability: ± 10 ppm / 0°C to 70°C is available

SPECIFICATIONS

Frequency Range	1 MHz to 125 MHz ($V_{cc} = 3.3\text{V}$), to 160 MHz ($V_{cc} = 5\text{V}$)
Input Voltage (V_{cc})	A = +5 VDC $\pm 5\%$; B = +3.3 VDC $\pm 5\%$
Input Current (Max.)	20 mA (to 20 MHz); 40 mA (to 40 MHz); 60 mA (to 100 MHz); 80 mA (to 160 MHz)
Control Voltage (V_c)	+2.5V $\pm 2.0\text{V}$ for 5.0V part; +1.65V $\pm 1.5\text{V}$ for 3.3V part
Storage Temperature	-55°C to 125°C
Frequency Stability / APR (Min)	A = $\pm 50 / \pm 50$ ppm; B = $\pm 25 / \pm 50$ ppm; C = $\pm 50 / \pm 100$ ppm; F = $\pm 10 / \pm 50$ ppm
Temperature Range	A = 0°C to 70°C ; B = -40°C to 85°C ; C = -10°C to 60°C
Standard Stability / Pullability	BA = ± 25 ppm / 0°C to 70°C , Absolute pull range (APR): ± 50 ppm Minimum
Duty Cycle	0 = No Tristate 60/40% symmetry; 2 = No Tristate 55/45% symmetry 4 = No Tristate 52.5/47.5% symmetry
Output Load	HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates
Logic "1" / Logic "0" Level	0.9 V_{cc} Minimum / 0.1 V_{cc} Maximum
Rise/Fall Time (T_r/T_f)	10 ns Maximum at 20% to 80% V_p -p
Start-up time	10 ms Maximum
Phase Jitter (RMS, 1 Sigma)	1 ps Maximum for $f_j > 1\text{kHz}$; 0.3 ps Typical for $f_j = 12\text{kHz}$ to 20MHz
Modulation Bandwidth	10 kHz Minimum at -3 dB
Linearity / Slope	$\pm 10\%$ Maximum of best straight line fit / Positive
Input Impedance	10 kOhms Minimum
Setability at F_{nom}, 25°C	+2.5V $\pm 0.5\text{V}$ for 5.0V part; +1.65V $\pm 0.4\text{V}$ for 3.3V part

Creating a Part Number



OUTLINE DRAWING

