

LVDS CRYSTAL OSCILLATOR IN CERAMIC LCC PACKAGE - XO53LVDS Series

FEATURES

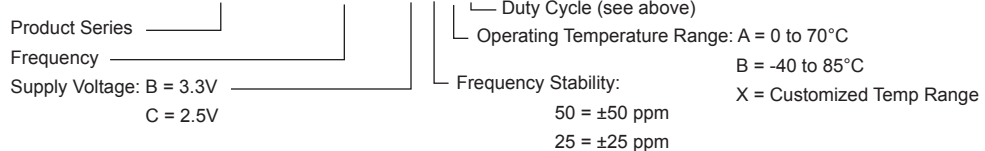
- RoHS Compliant (Pb-Free), LVDS Compatible Signals
- Inherent Low Power and Low EMI Emission
- Very Low Phase Jitter, No Internal PLL Avoids Cascading PLL Problems
- Complimentary Output, Tri-state Enable/Disable Standard, 5x3.2x1.4 mm SMD package

SPECIFICATIONS

Frequency Range	80 MHz to 270 MHz
Input Voltage (Vcc)	B = +3.3 VDC \pm 5%; C = +2.5 VDC \pm 5%
Input Current	66 mA Maximum, depending on frequency and output load
Storage Temperature	-55°C to 125°C
Overall Frequency Stability	50 = \pm 50 ppm; 25 = \pm 25 ppm
Temperature Range	A = 0°C to 70°C; B = -40°C to 85°C
Standard Stability	50A = \pm 50 ppm / 0°C to 70°C
Electric Option (Duty Cycle)	1 = Tristate 60/40%; 3 = Tristate 55/45%; 5 = Tristate 52.5/47.5% 0 = No tristate 60/40%; 2 = No tristate 55/45%; 4 = No tristate 52.5/47.5%
Output Load	100 Ohms across differential outputs (Offset 1.25V Typ)
Logic "1" / Logic "0" Level	1.43V Typ / 1.10V Typ
Rise/Fall Time (Tr/Tf)	0.7 ns Maximum at 20% to 80% Vp-p
Start-up time	5 ms Maximum
Phase Jitter (RMS, 1 Sigma)	0.3 ps Typical, 1 ps Maximum for fj = 12KHz to 20MHz
Phase Noise	-120 dBc/Hz at 1KHz, -140 dBc/Hz at 10KHz, -145 dBc/Hz at 100KHz
Tristate Function	Input (Pin 1) High (> 0.7Vcc) or open: Output (Pin 4, 5) active Input (Pin 1) Low (< 0.3Vcc): Output disabled in high impedance
Enable/Disable Time	2 ms Maximum - Enable; 200 ns Maximum - Disable

Creating a Part Number

XO53LVDS-155M520-B25B3



OUTLINE DRAWING

